REMARKS

Claims 1-28 are pending in this application. Claims 1, 7-8, 14-15, and 19 are independent.

Claims 1-28 stand rejected under 35 USC §103(a), as obvious over Hatano et al. (U.S. Patent No. 5,079,184), in view of Sasaki et al. (U.S. Patent No. 6,246,078). The rejections are respectfully traversed.

In the final Official Action of April 10, 2003 the Examiner maintains the rejection of claims 1-22 on the same grounds previously presented. As such, the traversal arguments presented in the responses filed on February 3, 2003 and January 14, 2002 are reasserted herein in their entirety. The Examiner is courteously requested to reconsider the aforementioned traversal arguments.

As discussed in previous responses, the present invention requires a p-type cladding layer, an insertion layer, and a p-type window layer. The required insertion layer prevents generation of a high potential barrier between the p-type cladding and the p-type window. As described in the present application at page 16, lines 3-7, the forward voltage can be lowered to 1.8V, as compared to the 2.4V forward voltage of a conventional LED by the claimed structure.

The Examiner's position that layer 47 shown in Figure 3 of Hatano is an insertion layer that "has all the characteristics" of the claimed insertion layer is unsupported. In particular, column 6, lines 5-14, of Hatano clearly recites that layer 47 is a clad layer

that serves as an etch stopping layer. In no place in Hatano is layer 47 described to be the required insertion layer.

Also, as repeatedly discussed in prior responses, a combination of Hatano and Sasaki, for which the Examiner has provided no motivation and for which it is respectfully submitted there is none, would not provide an insertion layer between a p-type cladding and p-type window layer which has a smaller band gap energy that the p-type cladding layer as required in claims 1, 7-8, and 14. The extent of the Examiner's arguments regarding Hatano teaching an insertion layer having a smaller band gap energy than a p-type cladding layer is the statement "this is shown". It is respectfully submitted that this requirement is not shown in Examiner-referenced Figure 3, nor is it disclosed in the text of Hatano.

Also lacking in a combination of Hatano and Sasaki is an insertion layer formed between a p-type cladding and a window layer (or in the p-type cladding), which is lattice-matched with and has a lower composition of Al than the p-type cladding layer and has a higher composition of Al than an active layer. Previously the Examiner argued that Hatano discloses lattice-matched layers without providing support for such argument. The Examiner now points to U.S. Patent No. 5,744,829, without making such of record, as teaching that, "the lattice constant of AlGaInP is to a high degree of precision only a function of the In content" and argues that "since all the layers of Hatano have the same In content they have the same lattice constant." It is respectfully submitted that, while the Examiner-referenced layers of Hatano may have the same In content, Hatano does not teach or suggest lattice-matched layers as required by certain ones of the present claims.

Claims 4, 11, 18, and 22 recite limitations on the range of the concentration of carriers in the p-type insertion layer. The Examiner again points to column 6, line 10, of Hatano as disclosing a carrier concentration. The referenced text discloses impurity concentration, not carrier concentration. The Examiner has yet to provide any rationale for a correspondence between the disclosed impurity concentration and the claimed carrier concentration.

The Examiner now notes that Sasaki shows carrier concentrations in the claimed ranges in layers 14, 15, and 17 of Figure 1A. Layer 14 is a cladding layer, layer 15 is an interface layer, and layer 17 is a current diffusion layer. None of these layers are the required insertion layer.

Regarding claims 7, 8, 14, 15, and 19, each of these claims requires an active layer which includes Al. Previously, the Examiner acknowledged that the active layer in Hatano "has no Al". As can best be understood, the Examiner has now reversed his position, though the Examiner does not identify where in Hatano such an active layer is disclosed.

Also, the Examiner has again failed to identify where in the Sasaki reference the window composition required in claims 7 and 14 is to be found.

Claims 15 and 19 require that the p-type window layer be doped with zinc. The Examiner has again failed to identify any disclosure within Sasaki which describes such a zinc doped window.

Claims 17 and 21 require that the p-type cladding layer be doped with zinc. The Examiner acknowledges that Hatano does not disclose a p-type cladding layer doped with Zn, but rather discloses a p-type cladding layer doped with Mg. The Examiner

looks to Sasaki for a Zn doped p-type cladding layer and argues that it would be obvious to substitute Sasaki's doping for Hatano's doping as a design alternative. The Examiner provides no support for his contention that the use of Zn rather than Mg is merely a design alternative.

Claims 23-28, each requiring that an insertion layer lower a forward voltage between a p-type cladding layer and a window layer, were added to the present application by the Amendment of February 3, 2003. The Examiner has failed to examine these claims, arguing that "functional limitations carry no weight in claims drawn to a device."

The Examiner's attention is respectfully called to section 2173.05(g) of the MPEP regarding functional limitations. The examination guidelines clearly require the Examiner to consider and properly examine functional limitations. Further, the Examiner's attention is called to R.A.C.C. Industries Inc. v. Stun-Tech Inc., 49 USPQ2d 1973 (CA FC 1998), as clearly holding that claims directed to a device or apparatus may include functional limitations. The Examiner is mistaken in arguing that functional limitations carry no weight in claims drawn to a device.

Because the Examiner has not considered and properly examined claims 23-28, the final rejection of at least claims 23-28 is improper. It is respectfully requested that the Examiner withdraw the improper final rejection of claims 23-28 and properly examine the same in light of his duties.

As previously discussed, the insertion layer can be used to lower the forward voltage from the 2.4V of a conventional LED to 1.8V. In this regard, Hatano discloses that the low voltage obtainable with the Figure 3 Hatano structure is 2.1V. The addition of a

window (as proposed by the Examiner) will typically result in an increase in this voltage. Thus, the requirements of claims 23-28 are neither taught nor suggested by Hatano, Sasaki, or a combination of the two.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed local telephone number, in order to expedite resolution of any remaining issues and further to expedite passage of the application to issue, if any further comments, questions or suggestions arise in connection with the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 01-2135 and please credit any excess fees to such deposit account.

Respectfully submitted,
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